INTERBUS

Conformance Test

Basic Test

General Section

Table of Contents

1. Introduction

This section of the specification for the INTERBUS conformance test describes the procedures for verifying the device by testing the test object (**E**quipment **u**nder **T**est - EUT) in the test installation, manual testing by the person carrying out the test, and through the manufacturer declarations.
The main issue is testing the relevant hardware and the behavior of the test object in an INTERBUS system. The minimum level of operation for INTERBUS components is also tested.
The selection of test tools and the test structure ensures that the test conditions for this group of INTERBUS master and slaves correspond to the majority of INTERBUS applications.

2. Test Objective

The aim of the test series is to determine by assessment, whether the test object can be operated correctly in a real INTERBUS system. The test object must also provide a minimum level of operation to be used practically by the user in an INTERBUS network.

3. Test Environment

3.1. Documents

In order to plan and carry out an INTERBUS conformance test, the user and installation manuals for the test object must be supplied by the manufacturer.

- Comprehensive documentation (user manual, data sheet, package slip, etc.) for the device
- Circuit diagram documentation
  Excerpts from the circuit diagrams which show the complete INTERBUS interface, including the peripheral connection, potential concept, and the power supply
- Associated component mounting plans
- Associated component parts lists and, if necessary, data sheets for components and the results of component tests, which have been used contrary to the recommendations given in the reference documents
- Device description in electronic form
- Necessary manufacturer declarations

All manufacturer documentation must correspond to the status of the series. It forms part of the test protocol and remains with the INTERBUS Club after successful certification.

The following up-to-date documents are also required:
- This conformance test specification with its various parts and appendices
- Description and user guide to software tools
- User manuals and reference circuit diagrams for the corresponding INTERBUS protocol chips

3.2. Test and Measurement Tools

The following are required for the basic test:

- Test tools from the applicant
- INTERBUS test structure
- "ENVI" test tool

3.2.1. Test Tools From the Applicant

In order to carry out the INTERBUS conformance test, additional equipment and devices are required from the manufacturer of the test object, which enable the following:

- Practical operation of the test object
- Triggering of required events for the test object

3.2.2. INTERBUS Test Setup

Different test setups are available for testing the various INTERBUS modules. These are described in the "Test Setups" appendix.

3.2.3. ENVI Test Tool

The ENVI test tool is used for the control, logging, and management of the tests and test object parameters.
The ENVI test tool also generates the test report.

The minimum hardware requirements for the test are an IBM-compatible PC with Windows NT and Generation 4 INTERBUS PC interface board.

For additional information, please refer to the ENVI test tool installation manual.

4. "Basic Test" Test Procedures

The basic test is divided into different groups according to the physical interfaces as follows:

- Remote bus/installation remote bus devices
- Devices with optical fiber interface
- INTERBUS Loop devices
- Local bus devices (Inline, etc.) (in preparation)

The baud rate used (500 kbaud/2 Mbaud) is not important for the individual test steps. However, the baud rate must always be specified so that the person carrying out the test can select the correct test setup.

INTERBUS slave devices, which have protocol chips with the diagnostic and report manager (SUPI 3, LPC 2, etc.) are required for the design check.
The reference circuit diagrams for the applications are the example circuit diagrams in the corresponding up-to-date user manuals for the protocol chips.
All "**HE**" test steps are implemented in the manufacturer declaration.
The test laboratory carries out "**TL**" test steps.
Where several options are available, a specific option must be selected.

4.0.1. Checklists for the Basic Test

All relevant checklists for the basic test are described below. The configuration data given in the conformance test application form determines which checklists are needed for a successful test.

4.0.2. Checklist Structure and Assessment Criteria

The "test steps" for the test object are described in the second column and the number of the relevant checklist is given in the first column. The person carrying out the test only has to enter the test result in the "OK" column. Any comments are entered in the "Note" field (fourth column). The assigned text appears at the bottom of the table as a footnote.

No.	Test Steps	OK

Figure 1: Checklist structure

The following applies to the assessment of the test steps:

Y Criterion met:

All specifications for this test step must be met.

Y- Criterion met - deviation permitted.
For deviations that influence neither the electrical response nor the time response of the interface, the person carrying out the test may positively assess this part of the test.
Example: Pull-down resistor of 3.3 kΩ instead of 2.7 kΩ was used.

N Criterion not met, deviation not permitted.

According to the person carrying out the test, the deviations influence the electrical or time response of the interface in such a way that the test step must be assessed negatively.

/ Criterion not to be taken into consideration.

The criterion does not apply to the test object and this test step is not relevant to the overall assessment.

For the overall assessment criterion to be "Passed", each test step must receive either the "Criterion met" or "Criterion met - deviation permitted" assessment. If deviations are detected, they must be noted and the final decision must be justified.

4.1. Physical Interface

No.	Test Steps	Section	OK
1.	What type of physical interface is used?		
2.	RS-485 interface (copper)	4.1.1	
3.	Optical fiber interface	Described in "Optical Fiber Basic Test"	
4.	INTERBUS Loop	Described in "INTERBUS Loop Basic Test"	
5.	Local bus devices (ST, Inline, etc.)	In preparation	

4.1.1. Remote Bus/Installation Remote Bus With RS-485 Copper Interface

This area is usually assessed by checking the circuit diagram. This is implemented in the manufacturer declaration. This area of the test is limited for the supplied circuit diagrams, because the cost of testing all relevant parameters is not justifiable.

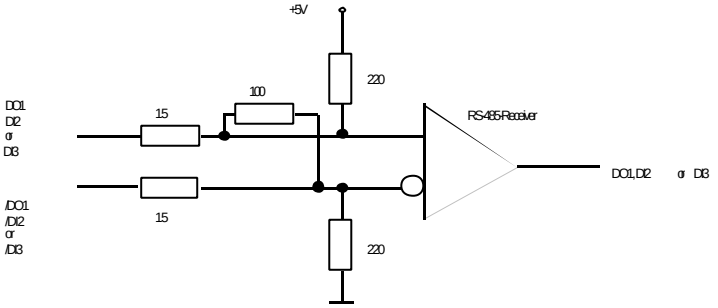
4.1.1.1. Driver, Optocoupler

No.	Test Steps	OK
1. **HE** 1.	**RS-485 driver/receiver** - Has an approved type or alternative *) been used with the specified circuit for the RS-485 driver/receiver in the INTERBUS data path? - Which? (please enter here)	

*) See table for approved components
Alternatively, the results of the component test in accordance with the INTERBUS Club specifications can also be submitted.

Approved Components:

Item No.	Designation		Manufacturer	Manufacturer's Designation
1.	IC 75176 B		TEXAS	SN 75176 BP
		SM	TEXAS	SN 75176 D
2.	IC AD 485		Analog Devices	ADM 485
		SM	Analog Devices	
3.	IC 75179 B		TEXAS	SN 75179 BP
		SM	TEXAS	SN 75179 BD
			TEXAS	SN 65179 BP
		SM	TEXAS	SN 65179 BD
		SM	TEXAS	SN 65LBC179
		SM	TEXAS	SN 75LBC179

No.	Test Steps	OK
2. **HE** 2.	**Polarization circuit diagram** - Has the polarization circuit specified in step "1" been implemented with 15 Ohm, 100 Ohm, 220 Ohm resistors as shown?  All resistors have a tolerance of +/-1%.	

No.	Test Steps	OK
3. **HE** 3.	**Optocoupler** - Has an approved type or alternative *) been used with the specified circuit for the optocoupler in the INTERBUS data path? - Which? (please enter here)	
4. **HE** 4.	- Does the series resistor in the LED circuit correspond to the value specified for the optocoupler?	
5. **HE** 5.	- Does the pull-up resistor at the output of the optocoupler correspond to the value specified for the optocoupler?	
6. **HE** 6.	- Is each optocoupler equipped with a 100 nF blocking capacitor?	

*) See table for approved components
Alternatively, the results of the component test in accordance with the INTERBUS Club specifications can also be submitted.

Item No.	Designation		Manufacturer	Man. Des.	$R_{I\ Diode}$	R_{PunOut}
6.	OPTOKOP.HCPL 0601	SM	HP	HCPL 0601	390 Ω ± 1%	390 Ω ± 1%
7.	OPTOKOP.HCPL 0611	SM	HP	HCPL 0611 new	390 Ω ± 1%	390 Ω ± 1%
8.	OPTOKOP.HCPL 2601		HP	HCPL 2601 old	390 Ω ± 1%	390 Ω ± 1%
9.	OPTOKOP.HCPL 2611		HP	HCPL 2611 new	390 Ω ± 1%	390 Ω ± 1%
10.	OPTOKOP.HCPL 2630		HP	HCPL 2630 old	390 Ω ± 1%	390 Ω ± 1%
11.	OPTOKOP.HCPL 2631		HP	HCPL 2631 new	390 Ω ± 1%	390 Ω ± 1%
12.	OPTOKOP.HCPL 4661		HP	HCPL 4661 new	390 Ω ± 1%	390 Ω ± 1%
13.	OPTOKOP.HCPL 2601		TI	HCPL 2601	390 Ω ± 1%	390 Ω ± 1%
14.	OPTOKOP.TLP 2601		Toshiba	TLP 2601	390 Ω ± 1%	390 Ω ± 1%
15.	OPTOKOP.HCPL061N	SM	HP	HCPL-061N	750 Ω...820 Ω	390 Ω ± 1% actual

4.1.1.2. Connection Method

No.	Test Steps	OK
1. **HE** 7.	**Connector pin assignment** - Has an approved type of connector with defined pinning (labeling, assignment, order of the connections especially for the terminals) been used? *) - Which? (please enter here)	
2. **HE** 8.	**Additional wiring** for INTERBUS data lines - Have any other active or passive components (e.g., Transsorb or suppressor diodes, filters, etc.) been used on/in the INTERBUS data path in addition to those listed?	

*) Approved connector types:
Alternatively, other connection methods can be selected. However, appropriate adapters must also be supplied as standard.

- D-SUB 9
- IP 65 circular connector
- Terminals
- Copper Rugged Line connector

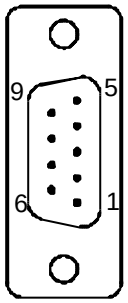
Explanations: see below.

4.1.1.2.1. D-SUB 9

Connector Pin Assignment

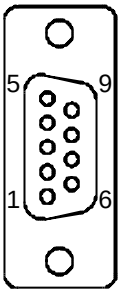
IP 20 Connector for Remote Bus (D-SUB9) and Device Side

Incoming interface
Solder side



D-SUB 9
Male connector

Outgoing interface
Solder side



D-SUB 9
Female connector

Pin	Standard	Option 1
1	DO1	DO1
2	DI1	DI1
3	GND1	GND1
4	n.d.	GND*
5	+5 V1*	+5 V1*
6	/DO1	/DO1
7	/DI1	/DI1
8	n.d.	+5 V*
9	n.d.	n.d.

Pin	Standard	Option 1	Option 2
1	DO2	DO2	DO2
2	DI2	DI2	DI2
3	GND	GND	GND
4	n.d.	n.d.	*GND**
5	+5 V	*GND*	+5 V
6	/DO2	/DO2	/DO2
7	/DI2	/DI2	/DI2
8	n.d.	n.d.	*+5 V**
9	RBST	*/RBST*	RBST

n.d. = not defined

* Optional for some optical fiber converters. This voltage does not have to be electrically isolated.

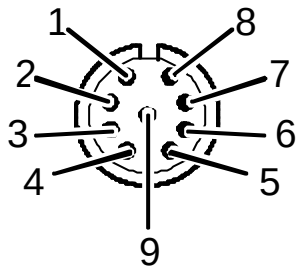
Note:
What applies to the outgoing interface also applies to any branch interface that is used.

4.1.1.2.2. IP 65 Circular Connector

IP 20 Connector for Installation Remote Bus (CCO-I) and Device Side

Incoming interface

Solder side

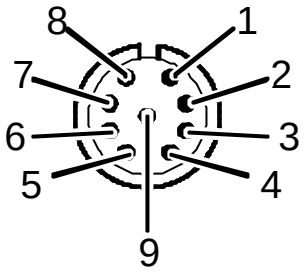


IP 65 circular connector
8+1-pos. male connector

Pin	Standard	Option 1 Installation Remote Bus
1	DO1	DO1
2	/DO1	/DO1
3	DI1	DI1
4	/DI1	/DI1
5	GND1	GND1
6	n.d.	FE
7	n.d.	+24 V
8	n.d.	0 V
9	n.d.	n.d.

Outgoing interface

Solder side



IP 65 circular connector
8+1-pos. female connector

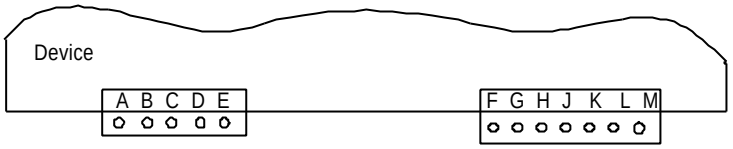
Pin	Standard	Option 1 Installation Remote Bus
1	DO2	DO2
2	/DO2	/DO2
3	DI2	DI2
4	/DI2	/DI2
5	GND	GND
6	n.d.	FE
7	n.d.	+24 V
8	n.d.	0 V
9	/RBST	/RBST

No.	Test Steps	OK
1. **HE** 9.	**24 V supply voltage loop** from input to output - All 3 signals FE, +24 V, and 0 V must be looped through without any additional elements (fuses, resistors, etc.) from the input to the output.	
2. **HE** 10.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Installation remote bus I_{Nom} = 4.5 A	

Note:
What applies to the outgoing interface also applies to any branch interface that is used.

4.1.1.2.3. Terminals

Remote Bus Connector (Screw-Clamp Terminals) for Device Side



Incoming interface Outgoing interface

Pin	Standard
A	/DO1
B	DO1
C	/DI1
D	DI1
E	GND1

Pin	Standard	Option 1	Option 2	Option 3 (Only for Automatic RBST Detection)
F	/DO2	/DO2	/DO2	/DO2
G	DO2	DO2	DO2	DO2
H	/DI2	/DI2	/DI2	/DI2
J	DI2	DI2	DI2	DI2
K	GND	GND	GND	GND
L	/RBST	RBST	Separate switch	
M	Unused	+5 V		

A separate FE terminal should be provided for the shield connection.
Warning: The order of the terminals must be maintained.

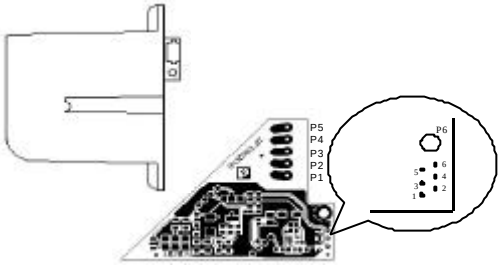
Note:
What applies to the outgoing interface also applies to any branch interface that is used.

4.1.1.2.4. Copper Rugged Line Connector

IP 65 Rugged Line Connector for Installation Remote Bus and Device Side

Incoming interface

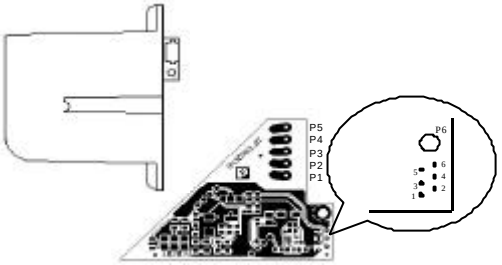
Solder side



Rugged Line male connector, 5+6-pos.

Outgoing interface

Solder side



Rugged Line female connector, 5+6-pos.

Female Connector Pin Assignment (Logic)	Pin	Wire Color
5 V supply	1	
Transmit data (analog output from OPC)	2	
GND	3	
Receive data (digital input from OPC)	4	
GND	5	
GND	6	
GND	P6	Shield
Signal (Power)	**Pin**	
+24 V US1 (bus/initiator supply)	P1	Brown
GND US1	P2	Blue
+24 V US2 (actuator supply)	P3	Red
GND US2	P4	Black
Functional earth ground	P5	Yellow/green

No.	Test Steps	OK
1. **HE** 11.	- All signals FE, +24 V, and 0 V must be looped through without any additional elements (fuses, resistors, etc.) from the input to the output.	
2 **HE** 12.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Rugged Line I_{Nom} = 16 A	
3 **HE** 13.	**Data connection from the Rugged Line connector** - The length of the shielded cable from the Rugged Line connector to the device electronics should not exceed 20 cm (7.87 in.).	
4 **HE** 14.	- Is the shield of the data connection cable for the Rugged Line connector connected to the GND on both sides?	

Note:
What applies to the outgoing interface also applies to any branch interface that is used.

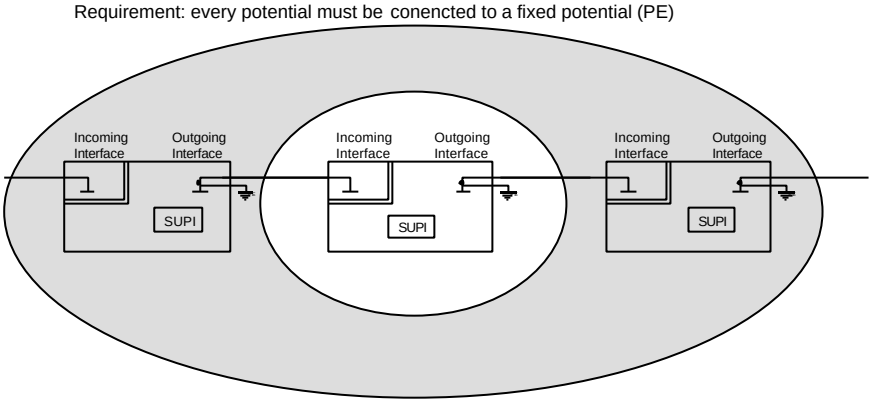
4.1.1.3. Potential and Shielding Concept

The following circuit diagrams should clarify the concepts discussed:

Circuit diagram for the prevention of floating potentials

Standard solution

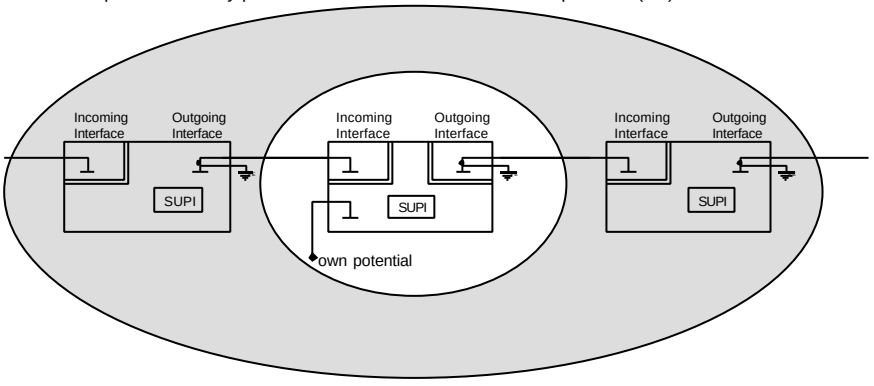
Requirement: every potential must be conencted to a fixed potential (PE)



Circuit diagram for the prevention of floating potentials

Optional solution

Requirement: every potential must be connected to a fixed potential (PE)

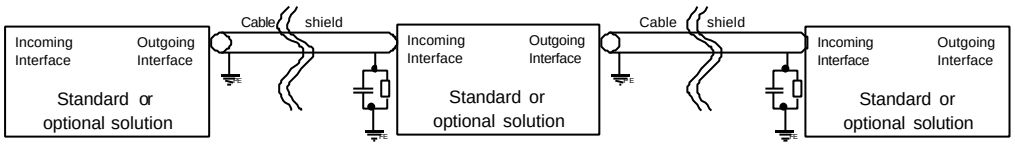


It is also possible to connect the GND of the outgoing interface with FE via a capacitor/resistor combination (C = 15 nF, R< = 1 Mohm), rather than directly to FE.

Circuit diagram to protect the INTERBUS system from EMD

Requirements: - Best derivation of the EMD
- No compensating current via the shield

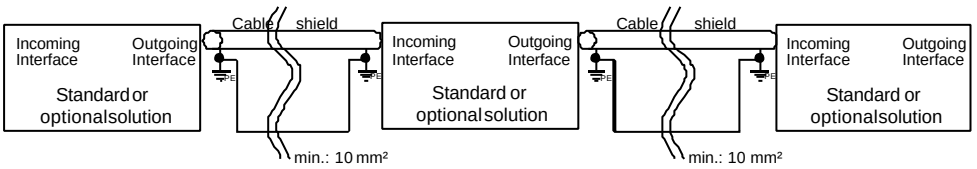
1. Solution: FE connection only on the outgoing interface, high frequency connection on the incoming interface



Circuit diagram to protect the INTERBUS system from EMD

Requirements: - Best derivation of the EMD
- No compensating current via the shield

2. Solution: Separate potential compensation, ∅ 10 mm² (8 AWG), minimum



No.	Test Steps	OK
1.**TL**	- FE connection - resistance measurement for disconnected device	
1.1. **TL** 1.	- Incoming interface measurement GND1 to FE; R > 1 Mohm	
1.2. **TL** 2.	- Incoming interface GND1 to 0 V of the device supply; R > 1 Mohm	
1.3 **TL** 3.	- Outgoing interface GND to FE; R = 0 Ohm *)	
1.4 **TL** 4.	- Optional, if available: Branch interface GND to FE; R = 0 Ohm *),	
2.**TL**	Shield connection - resistance measurements for disconnected but fully cabled device **)	
2.1. **TL** 5.	- Shield for incoming interface to FE; R approximately 1 MOhm***)	
2.2. **TL** 6.	- Shield for outgoing interface to FE; R = 0 Ohm *)	
2.3. **TL** 7.	- Optional, if available: Shield for branch interface to FE; R = 0 Ohm *)	
3.0 **HE** 15.	- The isolation voltage between the individual electrically isolated areas is at least 350 V AC.	

*) If FE of the outgoing interface is not directly connected with GND, a capacitor/resistor combination (R <= 1 MOhm, C approximately 15nF) (parallel circuit) can be selected as an alternative. **HE** 16.

**) The basic aim is to ensure a good shield connection with regard to EMC and to simultaneously prevent the flow of current (voltage equalization current) via the shield.

***) R = 0 Ohm permitted, if an equipotential bonding line of at least 10 mm² (8 AWG) between this device and the previous device is specified in the user documentation.

If the branch interface is a local bus, this is not tested because there is no definition available. (Comments)

4.2. Protocol Chip/Configuration/Wiring

No.	Test Steps	OK
1. **HE** 17.	**Protocol chip** - Has an approved type of protocol chip or an approved alternative been used? *)	
2. **HE** 18. **TL** 8.	- If the chip has optical control, is it disabled? (RF1=RF2=1 for SUPI3 OPC)	
3. **HE** 19.	- Are all the unused inputs for the protocol chip (including MFPs) connected with a defined voltage?	
4.a. **HE** 20.	**Applications with microprocessor interface:** - Is the "Microprocessor Not Ready" ID code set for the hardware? (at the ID pins (ID0 through ID7) or by a corresponding configuration specification on the slave protocol chip) Permitted ID codes: - 38_{hex} - For remote bus devices (standard) - 68_{hex} - For INTERBUS Loop devices (standard) - $3C_{hex}$ - For remote bus devices (for devices with special requirements, only is approved by the INTERBUS Club.)	
4.b **HE** 21.	- Supply device with voltage. - The microprocessor must be in a sate where it has not yet initialized the protocol chip. - During bus startup, the Generation 4 master reads in the "Microprocessor Not Ready" ID code and generates the "Incorrect initialization of the protocol chip by the microprocessor" error message 0C73 and 0D70 ..0D73	
5. **HE** 22.	- Place microprocessor in operating state. - The expected ID code can be read in after bus startup.	

*) See table for approved components

Item No.	Designation		Manufacturer	Manufacturer's Designation
1.	IC SUPI 3, PLCC84	SM	Motorola	GSC02AL373PI04
2.	IC SUPI 3, QFP100	SM	Motorola	GSC02AL373CE03
3.	IC SUPI 3, PLCC84	SM	ES2	
4.	IC SUPI 3, QFP100	SM	ES2	
5.	IC SUPI 3 OPC, QFP64	SM	ST	
6.	IC SUPI 3 BT, QFP64	SM	ST	
7.	IC SUPI 3 LS, QFP44	SM	ST	

4.2.8. Voltage Supply

No.	Test Steps	OK
1. TL 9.	Voltage supply - The device is supplied with a nominal supply voltage. - The device is started by the INTERBUS master. - The INTERBUS master then changes to RUN state. - The supply voltage is reduced until the green UL LED goes out. (The INTERBUS protocol chip should now switch to RESET state.) - A G4 master shows the error precisely and locates the device.	
2. TL 10.	Voltage supply - The supply voltage is increased slowly until the green UL LED lights up. (The voltage at the slave protocol chip must now be at least U_{Nom} minus the tolerance. The INTERBUS protocol chip should no longer remain in the RESET state). The master must be able to start up the bus system.	
3. TL 11.	Voltage supply - The INTERBUS master then switches to READY state. - The supply voltage is then reduced again until the green U_L LED goes out. The voltage is then increased again until the green U_L LED lights up. - The INTERBUS master then switches to ACTIVE state. An error message states that the device has run through a power-up reset.	

4.3. Reset Wiring (Slave Protocol Chips and Assigned Expansion Blocks)

No.	Test Steps	OK
1. **HE** 23.	- The power-up reset input of the slave protocol chip and the assigned expansion blocks are wired with a 1 kOhm, 100 nF filter.	
2. **HE** 24.	- The voltage monitoring circuit ensures that the reset input for the protocol chip and the assigned expansion blocks has a low signal with a voltage of U Nom minus the tolerance (5 V - 10%, typical).	
3. **HE** 25.	- The reset time realized by the voltage monitoring circuit is at least 2 oscillator clock cycles (125 ns at 16 MHz, typical) for the balanced oscillator and at specified voltage.	
4. **HE** 26.	- For direct and indirect wiring of the reset input, ensure that the components used in the entire voltage area of the voltage monitor are operating properly. Standard logic gates are **not** suitable.	
5. **HE** 27.	- The power-up reset of the slave protocol chip and the assigned expansion blocks is never influenced by the software, an LCA or microprocessor.	
6 **HE**	- Special consideration for IBS SUPI 3 OPC and SUPI3 OPC LS. This protocol chip family has a bi-directional pin with an open drain output, internal pull-up of 5..15 kOhm and a Schmitt trigger input (switching threshold 0.6 V ... 2.4 V). The output has a maximum load capacity of 8 mA. As a result the following apply in addition to the other points:	
6.1. **HE** 28.	- The resistance between +5 V and the reset pin of the IBS SUPI 3 OPC protocol chip family is **never** lower than 600 Ohm.	
6.2. **HE** 29.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an input: The resistance between GND and the reset pin of the protocol chip does not exceed 600 Ohm on a "0" signal.	
6.3. **HE** 30.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an output: The resistance between GND and the reset pin of the protocol chip is not less than 23 kOhm.	

4.4. Clockline

No.	Test Steps	OK
1. **HE** 31.	- A clock (e.g., quartz oscillator) applied at the protocol chip meets the requirements given in the INTERBUS protocol chip data sheet. **)	
2. **HE** 32.	- A quartz used meets the requirements given in the INTERBUS protocol chip data sheet. ***)	
3. **HE** 33.	- A quartz oscillating circuit does not supply other components with its clock.	
4. **HE** 34.	- The clockline is not influenced by other logic or software.	
5. **HE** 35.	- The clockline circuit is tested for the entire permissible temperature range of the device +/- 10%.	
6. **HE** 36.	- Additional capacitors for the IBS SUP13 quartz **OPC** quartz inputs are not available.	

*) The reset must not be controlled by a microcontroller or any other programmable logic, because software errors, etc. could then interfere with bus operation.
**) Typical: f=f_{Nom}+/- 100 ppm, 50% duty cycle, short and long-term stability
***) Typical: Quartz f_{Nom} +/- 100 ppm, C_L; R_{Seq}, 50% duty cycle, short and long-term stability

4.5. Register Expansion (Optional)

No.	Test Steps	OK
1. **HE** 37.	**Register expansion (optional)** - Have approved types or an approved alternative been used for the expansion blocks? *)	
2. **HE** 38.	- One data output for the register expansion does not drive more than 4 inputs.	
3. **HE** 39.	- If a buffer is used for the register expansion signal ClkExR, have identical buffers been used for signal ToExR2?	
4. **HE** 40.	- Are the register expansion registers in close proximity to the protocol chip on the same board? The tracks are < 5 cm (1.97 in.).	
5. **HE** 41.	- Are the Latch, Data (IN&OUT), Clock, and /ResReg signals for the register expansion blocks only used by the INTERBUS slave protocol chip or by the reset logic that controls it?	

*) See table for approved components
Alternatively, the results of the component test in accordance with the INTERBUS Club specifications can also be submitted.

Item No.	Designation		Manufacturer	Manufacturer's Designation
16.	IC 74 HC 164		HARRIS TEXAS	CD 74 HC 164 E SN 74 HC 164 N
17.		SM SM	PHILIPS MOTOROLA	PC 74 HC 164 T MC 74 HC 164 D
18.	IC 74 HCT 164		HARRIS NATIONAL PHILIPS	CD 74 HCT 164 E MM 74 HCT 164 N PC 74 HCT 164 P
19.	IC 74 HC 165		HARRIS	CD 74 HC 165 E
20.		SM SM SM SM SM	HARRIS PHILIPS SGS-THOMSON TEXAS NATIONAL	CD 74 HC 165 M PC 74 HC 165 T M 74 HC 165 M1 SN 74 HC 165 D MM 74 HC 165 M
21.	IC 74 HCT 165		HARRIS PHILIPS	CD 74 HCT 165 E PC 74 HCT 165 P
22.	IC 74 HC 594		TEXAS NATIONAL	SN 74 HC 594 P MM 74 HC 594 P
23.		SM SM	TEXAS NATIONAL	SN 74 HC 594 D MM 74 HC 594 D
24.	IC 74 HC 595		TEXAS MOTOROLA MOTOROLA	SN 74 HC 595 N MC 74 HC 595 N MC 74 HC 595 AN
25.		SM SM	TEXAS VALVO	SN 74 HC 595 D PC 74 HC 595 TP
26.	IC 74 HCT 595		TEXAS NATIONAL	SN 74 HC 595 P MM 74 HC 595 P
27.		SM SM	TEXAS NATIONAL	SN 74 HC 595 D MM 74 HC 595 D
28.	IC 74 HC 597		TOSHIBA SGS-THOMSON HARRIS NATIONAL HITACHI MOTOROLA	TC 74 HC 597 AP M 74 HC 597 B1N CD 74ACT258 E MM 74ACT258 N HD 74ACT258 P MC 74ACT258 N
29.	IC 74 HCT 597		PHILIPS HARRIS	PC 74 HCT 597 P CD 74 HCT 597 E
30.	IC IBS SRE 1		Phoenix Contact	IBS SRE 1

4.6. Diagnostics

4.6.1. Diagnostic LEDs

No.	Test Steps	OK
1. **HE** 42.	**Diagnostic signals** - The required diagnostic LEDs for this device type (see table) are directly connected to the slave protocol chip and are not controlled via software (with the exception of TR). *)	
2. **HE** 43.	- The green U_L LED is directly controlled by the voltage monitor.	
3. **TL** 12.	- The color and labeling of the diagnostic LEDs correspond to the specifications. **)	
4. **TL** 13.	- The order of the diagnostic LEDs corresponds to the order specified. ***)	
5. **TL** 14.	- If the INTERBUS diagnostic information is also displayed on the device (e.g., on a display), this display does not contradict the status of the LEDs. For example, an unlit RC LED cannot be displayed as "INTERBUS Error" in the display.	
6. **TL** 15.	Check the function of the diagnostic LEDs.	

4.6.2. Diagnostic Options

No.	Test Steps	OK
1. **HE** 44. TL 16	- If the protocol chip diagnostic input *I/O Error* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by these diagnostic messages are simulated and the response is checked at the INTERBUS master. ****) The data pattern 0xF0 is output for all OUT data bytes of the test object. This means it is also possible to test module error messages by short-circuiting a digital output.	
2. **HE** 45 TL 17	- If the protocol chip diagnostic input *Reconfiguration Request* ("Conf" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
3. **HE** 46 TL 18	- If the protocol chip diagnostic input *MAU Warning* ("MAUWS, MAUWR, MAUWH" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
4. **HE** 47 TL 19	- If the protocol chip diagnostic input *Microprocessor Watchdog* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
5. **HE** 48 TL 20	- If the protocol chip diagnostic output *Alarm* ("Alarm" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
6. **HE** 49	- If the protocol chip diagnostic output *Module Acknowledge* ("/ModAck" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
7. TL 21.	- Are all the subsequent events and resultant actions for all the diagnostic signals and their handling by the application accurately described in the user documentation?	

*) If the device uses PCP communication, each TR LED for PCP communication (transmitting and receiving PCP PDUs) must be lit so that it is **clearly visible**.

**) The diagnostic LEDs UL, RC, BA, RD, (TR) that were specified in the design check are part of the mandatory implementation and must be available in each device for servicing reasons. They do not have to be directly visible from the outside, although this may be desirable. It is sufficient that they are visible when the cover, service flap or similar is removed.
The TR LED - and only this LED - can also be controlled by software. The LED must light up in the event of a PCP send or receive interrupt. If another event is signaled and neither of these two sources is set, the LED must switch off again, after a maximum of 1 sec. (see above).

***) The diagnostic LEDs must be in the following order "UL, RC, BA, RD, (TR)" to ensure straightforward assignment for all INTERBUS devices (i.e., multi-tier/row from left to right and top to bottom).

****) All diagnostic signals are not designed for fast or cyclic signal exchange and should not be used for this.

Table: Device type and required diagnostic inputs/outputs
The order corresponds to the required order for the LEDs

Designation Color	**U_I** U-Mon. Green	**CC/RC** (/ResReg) Green	**BA** BA Green	**RD** (RBDA) Yellow	LD (LBDA) Yellow	TR (LBDA/TR) Green	FO1 FO2 (FO3) Yellow	**D** Diag Green	/Stat Err -	/Mod Ack -	Conf -
Operating mode											
Bus terminal module	M	M	M	M	M	-	O	O	O	O	M
Input/output	M	M	M	M	-	-	O	O	O	O	O
PCP device	O	O	O	O	-	M	O	O	O	O	O
Optical fiber device	M	M	M	M	-	O	M	O	O	O	O
IBS Loop device	O	O	O	O	-	O	-	M	O	O	O

M = Mandatory, **O =** Optional

LED Status Description

LED	Meaning
UL	Reset Protocol chip is/is not supplied with power.
RC/CC Remote bus Check Cable check	Communication Ready Communication to the IBS Master is/is not possible, the application has not yet started data exchange.
BA Bus active	Communication Active or Run Master active/no user data is exchanged. If the LED is flashing, communication from the INTERBUS master is not possible and the system operation is being monitored.
RD Remote bus disabled	Remote Bus Disabled The outgoing interface is/is not disabled.
LD - optional Local bus disabled	The branching interface is/is not disabled. Only for bus terminal modules.
TR- optional Transmit/receive	This is active for devices with PCP communication.
FO1 FO2 FO3	Fiber Optic Warning This LED (one per INTERBUS interface) indicates if the optical power for the corresponding receiver is too low in the **"Run"** operating mode.
Diag	INTERBUS diagnostic LED For the meaning of the flashing frequencies, please refer to the table.

Meaning of the Flashing Frequencies for the Diagnostic Signal:

State	Meaning
Static low signal (LED: dark)	The protocol chip is not supplied with sufficient power.
0.5 Hz clock with even pulse/pause ratio (LED: flashing at 0.5 Hz)	The protocol chip is supplied with voltage. The input ResU Reset is not active. Communication is not active.
2 Hz clock with even pulse/pause ratio (LED: flashing at 2 Hz)	An error status is detected at the input /StatErr. The protocol chip is supplied with voltage. Reset is not active. Communication is active, but it is not necessary to transmit valid data telegrams.
4 Hz clock with even pulse/pause ratio (LED: flashing at 4 Hz)	The protocol chip is the diagnostic master and generates telegrams, which are necessary for the detection of physical interrupts in the INTERBUS Loop ring. Data transmission is suspended.
Static high signal (LED: steady light)	This state indicates a layer 2 activity. Commination is active, valid data telegrams are transmitted. The protocol chip is supplied with voltage. Reset is not active.

4.7. Product Entry in the Supplier Index

TL 22.

A comprehensive device description is required from the outset for the conformance test. Information about the ID code, data length, interface type, etc. is compared with the data from the test configuration.
The device description(s) is/are generated in CMD (Version 4.50 or later) and exported from there as a database.
This database with the manufacturer's device description is submitted to the certification committee together with other documents, for entry in the INTERBUS Club database. (Send by floppy disk or e-mail to germany@interbusclub.com)

The device description data is checked as part of the basic protocol test.

4.8. Configuration

TL 23.

The configuration is checked in the basic protocol test. The test object must be operational in the test installation.
The ID code provided in the documentation must be identical to the one that is read in and must be compatible with the device according to the INTERBUS Club ID code specification (see appendix). To detect possible configuration problems for microprocessor circuits, the ID code is read in 10 times in succession (a bus reset is generated before each reading).

4.9. The Last Device

TL 24.

This test is used to check whether the outgoing INTERBUS interface (or the branch interface, if used) is closed when the connector is removed.

The bus configuration is read once the connector has been disconnected properly and is then compared with the remaining desired configuration. The connector should then be properly reconnected. After the bus has been reconfigured, the original bus configuration should be read once again.

4.10. Testing the Behavior of an Optional Power Unit

TL 25.

- Disconnection of the optional power unit when the bus is running.
- The bus continues to operate without any errors. I/O error messages or device indications are desirable but not essential.

4.11. Master <--> Test Object Data Transfer

TL 26.

Due to the variety of test objects, it is not possible to suggest specific data patterns. The person carrying out the test should use his or her own judgment to transmit data, reread it, and check the validity of the bits as often as required. It is the responsibility of the person carrying out the test to decide whether or not the test has been passed.

All IN and OUT data words for the test object are displayed. A maximum of 32 data words is specified for the test program. The IN data is constantly updated. At the same time, it is possible to modify all the OUT data of the test object. This OUT data is not immediately valid, however, because data consistency must be maintained for at least one word. The person carrying out the test must decide when the OUT data should be transmitted on the bus. The OUT data is displayed in reverse order. After a brief delay, the IN data is read in cyclically. Using this type of "monitor", devices such as frequency inverters may also be activated.

4.12. Basic Test for PCP

The basic PCP test is a short PCP test within the framework of the basic protocol test, which is designed to complement, rather than replace, the PCP test. The basic functions are tested on defined test objects provided by the manufacturer.

No.	Test Steps	OK
1. TL 27.	- During PCP communication the TR LED is clearly visible. This signal may be influenced by the microprocessor.	
2. TL 28.	- Using a faulty "initiate" service, the services, buffer lengths, and other settings implemented in the test object are determined and compared with the manufacturer data (defined PDU sizes, supported services).	
3. TL 29.	- Connections are established with the correct parameters and all permissible functions are implemented (including mandatory functions, e.g., reject and abort with reconnection without any errors) on the test objects with the permissible parameters. - The results are compared with the manufacturer's data. (Contents of the objects, status, identification)	
4. TL 30.	Continuous test - The continuous test should reveal errors during implementation caused by pointer or buffer overflow. The following cycle N=100 times is repeated. /* Begin */ - Establish connection Write test object 100 times - Read test object 100 times Write, read test object 100 times - Abort connection - 100 times - Establish connection - Write, read test object - Abort connection /* End */ User-defined errors may be accepted. This test is carried out at the same time as the EMC continuous test to save time. Cycles N*[400*Max_PDU_Size + 202*64] approximately 11 million cycles (6h)	
5. HE 50.	**Additional PCP error codes** - Additional PCP error codes defined by the manufacturer are always assigned error class "8", error code "0" in the additional code.	

Test Objects:

The index is specified by the manufacturer. Additional test objects should only be created if none of the existing objects can be written continuously without consequences for the rest of the basic PCP sequence.

Test object (only for PCP devices)

Name	Type	Index	Length

This table is to be completed by the manufacturer and submitted to the test laboratory for the conformance test.

5. Options

TL 31.

All options that have been implemented must function correctly.