INTERBUS

Conformance Test

Noise Immunity Test

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1 Introduction

This section of the specification for the INTERBUS conformance test describes the procedures for verifying the testing of the test object (**E**quipment **u**nder **T**est - EUT) in the test installation for the device.
The main topic addressed is testing the relevant hardware and the performance of the test object in an INTERBUS system.
A test procedure has been developed in a defined test environment as a result of years of practical experience and product observance, which ensures justifiable costs and a great deal of practical relevance.
This is why the INTERBUS external noise immunity test is suited to the relevant standards, itself defining conditions, guidelines, and requirements that must be met. This ensures greater comparability of test results and uncovers a high percentage of interferences, which actually occur in industrial systems.
The INTERBUS external noise immunity test does not however replace any complete test for the issue of a CE mark.

2 Aims of the Noise Immunity Tests

Noise immunity is classed as an essential requirement for electrical components that have a resistance to the effects of electromagnetic interference. During the INTERBUS conformance test, the record for the resistance of the prototype to system-specific influences and external system influences on the prototype is accurately tested and quantitatively proven.
The aim of this test is to ensure that the test object can function efficiently when the strain limit values are affected. The effectiveness of the EMC measures implemented is also tested.

2.1 Testing Internal Noise Immunity

Indicating the noise immunity of a device to internal influences is only possible indirectly. An additional function test must be carried out in extreme environmental conditions, i.e., for extremely tolerant power supply parameters used with the corresponding implementation class limit temperatures of the device. This means that the function interrupts in the test allow conclusions to be drawn about EMC weaknesses. Because individual results are targeted, the test object must be carefully protected from uncontrollable external influences during the test. Because noise immunity is an essential requirement for the functionality of the device, this point is not expanded upon in the INTERBUS conformance test. This is where the conscientiousness of the manufacturer is relied upon.

2.2 Testing External Noise Immunity

The aim of the external noise immunity test is to discover if and to what extent a device can resist interference of a specific type and intensity without malfunction. This is usually carried out within the framework of a function test in the laboratory. Anticipated interferences are reproduced by interference simulators connected on site and to defined device interfaces. This applies to conducted interference, which may find its way through the network connection, supply voltage connection, the bus inputs and outputs or the housing, and also applies to field related interference.

Various standards and regulations form the basis for testing external noise immunity. These regulations have been adapted and tightened for EU harmonization. All devices new to the market must meet these standards. This also means that each manufacturer is required to ensure that their device is electromagnetically mapped. Nevertheless, an EMC test based on the conformance test should be carried out according to IEC 61000-4-4.

Years of experience have shown that devices that have met the cited standards and have at least fulfilled the criteria of the external noise immunity test intensity level 3, and reaction to their use in the field has been positive. If devices are used that do not meet the requirements of the test class, this may lead to system failure in extreme conditions.

3 Definitions

The terms used in this test specification are defined below.

3.1 Operating State

The operating state refers to the test object in normal operation, i.e., if the user environment is integrated, it must be fully functional. Data is read in and out via the process channel in all INTERBUS devices. Devices that generate their own electromagnetic field in the operating state must be operated in such a way that the maximum noise emission level is reached. For example, for an electronically controlled drive this means that the connected drive can be used at the maximum positive speed of the test setup and can switch to the maximum negative speed after standstill (if possible). The speed is modified in 10 second intervals.

3.2 Data Error

A non-permissible modification to the incoming or outgoing data pattern connected to the test object or the monitoring modules (outputs from a module connected directly to the inputs of a second module).

3.3 System Failure

This refers to any state that is not permitted by the INTERBUS master within the system monitoring time or even the implementation of a valid data cycle. The INTERBUS master reacts to such fatal errors by carrying out a reset of all the connected modules.

3.4 Single Error

A single error means that the system has detected an interrupted bus cycle (single error), e.g., by comparing the CRC rest poliminals, and repeats the corresponding cycle automatically without external influence. However, this is only permitted up to a defined percentage of single errors.

4 Test Environment

4.1 Documents

In order to plan and carry out an INTERBUS external noise immunity test, the user and installation manuals for the device must be provided by the manufacturer.

- Comprehensive documentation (user manual, data sheet, package slip, etc.) for the device

Up-to-date versions of the following documents are also required:

1. The international standard "Electromagnetic compatibility for industrial-process measurement and control equipment, Part 4; Electrical fast transient requirements"; IEC 61000-4-4
2. This test specification for the INTERBUS conformance test - external noise immunity test
3. Measurement protocol forms as listed in the appendix (as long as no protocols are automatically set).
4. Description and user guide to software tools

4.2 Test and Measurement Tools

The following are required for the external noise immunity test:

- Test tools from the applicant
- Interference generator
- INTERBUS test structure
- "ENVI" test tool

4.2.1 Test Tools From the Applicant

In order to carry out the INTERBUS external noise immunity test, additional equipment and devices are required from the manufacturer of the test object, which enable the following:

- Practical operation of the test object
- Triggering of required events for the test object

4.2.2 INTERBUS Test Setup

Different test setups are available for testing the various INTERBUS modules. These are described in the "Test Setups" appendix.

4.2.3 ENVI Test Tool

The ENVI test tool is used to aid control, configuration, and management of the test and test object parameters.
The ENVI test tool also generates the test report.
The hardware needed for the test comprises at least an IBM-compatible PC with Windows NT operating system and an INTERBUS PC Generation 4 interface board. A Compaq device is recommended against the effects of interference.
Further details may also be found in the ENVI test tool installation manual.

4.2.4 Interference Generator

The following test and measurement tools are required for carrying out the external noise immunity test.

1. Generator for simulating low-energy transient interference voltages for bursts, e.g., EFT5 from EMTEST
2. RS-232 converter for coupling the burst generator to the control PC (optional)
3. Capacitative coupling clamp
4. 24 V mains device(s), linear control

5 External Noise Immunity Test Procedures

5.1 General Information About the Test Procedures

All possible test procedures for the external noise immunity test are described below. There are different procedures for the voltage inputs, bus inputs and outputs and a long-term test.
The design of the interference measuring area and the general conditions for the implementation of a noise immunity test are detailed in the standard specified and are therefore not given here. With regard to the objective comparability and safety of the reproducibility of the test results, the noise immunity tests are carried out according to the requirements specified in the standard. Photographs are also included with the test object to reproduce the test setup more accurately. The following points must be noted:

1. Adhere to the climatic environmental parameters.
2. Ensure special electrical environmental conditions.
3. Electrical parameters for interference generators, such as internal resistance, tolerance ranges, etc.
4. Electrical and constructive parameters for the coupling clamp.
5. Geometric location, cabling and grounding of the test devices and the test object.

It is essential that a bit pattern is statically set for the test object, to ensure that data errors are detected during the nose immunity test. The control PC must be able to read the bit pattern via the process channel. The test object must be remotely set to the operating state via the process channel. The manufacturer must supply all the necessary data. Alternatively, the manufacturer may provide an initialization and setup routine in C source code. The test sequence is carried out almost automatically. A program is used for this. The startup routine from the manufacturer and readable desired bit pattern are compiled in a single batch. After starting the program a noise immunity test either of the bus inputs and outputs or of the voltage inputs can be selected. For the first option, either a short or long-term test can be selected. The program counts the total and all faulty INTERBUS cycles. The bit pattern provided is usually compared to the one that is currently being read and any deviations are recorded. After the test time the counter readings are imported to the log and the next interference parameter is set for the burst generator. The next measurement is then started.
If the appropriate requirements are provided, the generator is set and the protocols from the ENVI test tool are implemented.

5.1.1 Test Steps

1. Structure and connection of the test object according to IEC 61000-4-4.
2. Batch compilation of the EMC test program with the test object parameters.
3. Test run with the connected burst generator.
4. Setting the test interference parameters at the burst generator according to the specified values.
5. Beginning the test step by starting the EMC test program.
6. Monitoring the test object and recording its reactions under the influence of interference. The noise immunity test is either cancelled or continued depending on the reactions.
7. Setting the protocols for the test sequence.
8. Steps 4 to 7 are repeated until the test must be interrupted or the final test interference parameter has been implemented.
9. Evaluation of the test results and generation of the test report.

Steps 4-9 are automatically carried out by the ENVI test tool.

5.1.2 Assessment Criteria

The external noise immunity test is "Passed" if the following criteria are met:

1. **No** data errors occurred in the specified voltage areas during the entire test (including the final value).
   (Evaluation criterion A)
2. The effect of the interference voltage did **not** lead to a system error during the entire test (including the final value).
   (Evaluation criterion A)
3. **No** data errors occurred in the specified voltage until the half-final value.
   (Evaluation criterion A)
4. A maximum of 1% single errors (5% single errors for INTERBUS Loop) occurred in the specified voltage areas when testing the half-final value to the final value of the test voltage.
   (Evaluation criterion B)

Note:

For a noise immunity test in accordance with IEC 61000-4-4 (well suited to the INTERBUS conformance test) with an intensity level of 4, criterion "B" must be attained, and for a test with an intensity level of 3, criterion "A" must be attained.
An intensity level of 4 is equivalent to ambient class 4 "Highly industrial environment" and an intensity level of 3 is equivalent to ambient class 3 "Typical industrial environment".
Criterion "B" means that a temporary reduction or failure of a function or a predetermined operation is restored by the device itself. With INTERBUS, the system recognizes an interrupted bus cycle (single error) and repeats the corresponding cycle automatically without external influence. However, this is only permitted up to a defined percentage of single errors.
Criterion "A" means a predefined operation within the fixed limits, therefore no single error with regard to INTERBUS (or only within the specified bus quality).

5.2 External Noise Immunity Test for Voltage Inputs

There are two options for the interference coupling in the noise immunity test for voltage inputs. In the first option bursts can be transmitted to the supply lines by a coupling clamp. In the second option a coupling network can be integrated as in EFT5 for a maximum voltage supply of 220 V. Only the coupling network is used for the INTERBUS conformance test. The following parameters apply to the test sequence:

Rise time for individual pulses:	5 ns +/- 30%
Pule duration:	50 ns +/- 30%
Burst lengths:	15 ms +/- 20%
Burst period:	300 ms +/- 20%
Burst frequency	5 kHz
Test voltage polarity:	Positive
	and negative
Test duration:	1 min
Number of tests:	1 per test voltage, polarity, and connection type
Test voltage:	
For nominal voltages < 60V	0.2 kV to 2.2 kV in 200 V steps
For nominal voltages > 60V	0.4 kV to 4.4 kV in 400 V steps
Interference coupling:	Via coupling network (Figure 1) a) symmetrical b) unsymmetrical c) asymmetrical
Effect of interference on the cable(s)	Supply lines • L1 (L2, L3) or + • N or - • FE

Operating conditions for the test object: operating state in the network

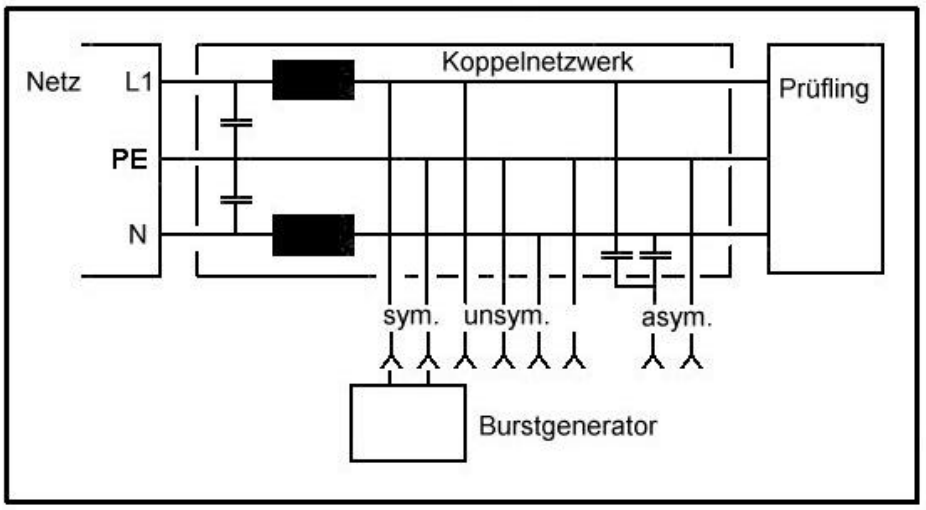

Fig 3: Coupling of burst pulses in power supply lines

Measuring protocols A1 and A2 are provided in the appendix for setting the protocols of the noise immunity test. Any unusual occurrences, such as flashing LEDs, faulty inputs/outputs, etc. are recorded in the test report, and on an additional page if necessary.

5.3 External Noise Immunity Test for Bus Inputs and Bus Outputs

Bus inputs and outputs are made by the indirect interference coupling via the coupling clamp during the noise immunity test. A test order is then established for the bus inputs. A second test order is then established for the bus outputs. The following parameters apply to the test sequence:

Rise time for individual pulses:	5 ns +/- 30%
Pule duration:	50 ns +/- 30%
Burst lengths:	15 ms +/- 20%
Burst period:	300 ms +/- 20%
Burst frequency	5 kHz
Test voltage polarity:	Positive and negative
Test duration:	1 min
Number of tests:	1 per test voltage, polarity, and connection type
Test voltage:	0.2 kV to 2.2 kV in 200 V steps
Interference coupling:	Via coupling clamp
Effect of interference on the cable(s)	• Bus inputs • Bus outputs (2, maximum)

Operating conditions for the test object: operating state in the network

Measuring protocol B is provided in the appendix for setting the protocols of the noise immunity test. Any unusual occurrences, such as flashing LEDs, faulty inputs/outputs, etc. are recorded in the test report, and on an additional page if necessary.

5.4 External Noise Immunity Test for Inputs and Outputs for I/O Devices

Inputs and outputs for I/O devices are made by the indirect interference coupling via the coupling clamp during the noise immunity test.
The following are possible I/O data signals:

- 24 V inputs
- 24 V outputs
- Analog inputs
- Analog outputs
- Serial inputs and outputs (RS-232, RS-485, etc.)

In order not increase the time and cost of the test unnecessarily, several inputs/outputs are selected per channel for each group in their usual connection type as an example for the test. The channel that is assumed to have the least cost-effective operation is selected.
The following parameters apply to the test sequence:

Rise time for individual pulses:	5 ns +/- 30%
Pule duration:	50 ns +/- 30%
Burst lengths:	15 ms +/- 20%
Burst period:	300 ms +/- 20%
Burst frequency	5 kHz
Test voltage polarity:	Positive and negative
Test duration:	1 min
Number of tests:	1 per test voltage, polarity, and connection type
Test voltage:	0.2 kV to 2.2 kV in 200 V steps
Interference coupling:	Via coupling clamp
Effect of interference on the cable(s)	Also inputs and outputs for I/O devices

Operating conditions for the test object: operating state in the network

Measuring protocol C is provided in the appendix for setting the protocols of the noise immunity test. Any unusual occurrences, such as flashing LEDs, faulty inputs/outputs, etc. are recorded in the test report, and on an additional page if necessary.

5.5 Long-Term External Noise Immunity Test

With regard to the setting the interference parameters, the same conditions apply as in the previous section for the external noise immunity test. The test procedure that yields the worst results is selected here. The total of single errors is decisive for a test.

Rise time for individual pulses:	5 ns +/- 30%
Pule duration:	50 ns +/- 30%
Burst lengths:	15 ms +/- 20%
Burst period:	300 ms +/- 20%
Burst frequency	5 kHz
Test voltage polarity:	Positive and negative
Test duration:	300,000 cycles
Number of tests:	1 per test voltage, polarity
Test voltage:	a) Mandatory range: 1 kV and 2.0 kV b) Optional area: 3.0 kV 4.0 kV 0.1 kV underneath the single error limit 0.1 kV above the single error limit
Interference coupling:	See corresponding test procedure *)
Effect of interferences on the cable(s)	See corresponding test procedure *)

Operating conditions for the test object: operating state in the network

The measuring protocol is provided in the appendix for setting the protocols of the noise immunity test. Any unusual occurrences, such as flashing LEDs, faulty inputs/outputs, etc. are recorded in the test report, and on an additional page if necessary.

*) The test procedure that yields the worst results is selected here. The total of single errors is decisive for a test.